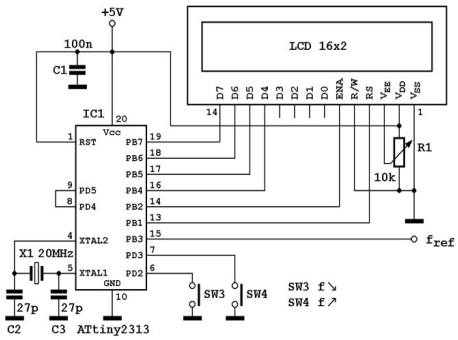
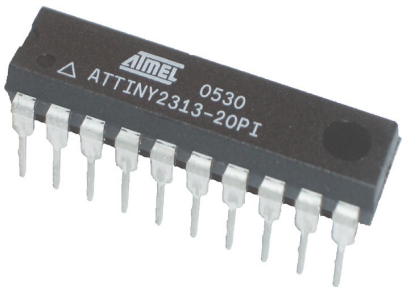


The ATtiny2313-based frequency reference produces a series of rectangular pulses with a 50% duty cycle. The frequency of these pulses is very stable, while the frequency range covers a full 10 decades, ranging from 0.001 Hz to 10 MHz.

Basic methods of frequency generation



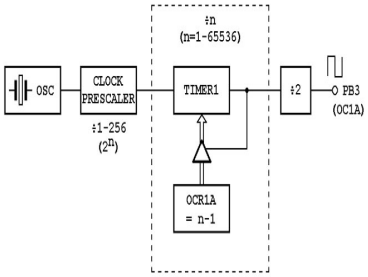
The circuit shown in Figure 1 is very simple, because everything is done inside the microcontroller. A 20 MHz quartz crystal is used as the microcontroller's clock source to allow the highest possible upper frequency limit. The clock frequency is divided inside the microcontroller by various division factors, to obtain the range of output frequencies mentioned above. As all the output frequencies are obtained strictly by frequency division, they are as stable and accurate as the crystal is.

The following microcontroller resources are used for frequency division:

- The 8-bit system clock prescaler divides the system clock by division factors of 1, 2, 4, 8, 16, 32, 64, 128 or 256. This affects the CPU clock and thus slows down the program execution proportionally.
- The 10-bit prescaler module divides the actual system clock by 1, 8, 64, 256 or 1024 for Timer/Counter0 and Timer/Counter1. The two Timers/Counters can have different prescaler

settings.

-



Timer/Counter0 counts the appropriately prescaled system clock pulses in Clear Timer on Compare (CTC) mode. In this mode, the counter is cleared to zero when its value matches the value in the OCR0A register. If the value in the OCR0B register is the same as the value in OCR0A, and the Timer/Counter has been properly configured, the output OC0B (PD5) will toggle whenever the counter is cleared. Values between 0-255 in the OCR0A and OCR0B registers will result in division factors of 2-512.

- Timer/Counter1 counts the appropriately prescaled system clock pulses in CTC mode. The counter is cleared to zero and the output pin OC1A (PB3) toggles whenever the counter value matches the value in the OCR1A register. Values 0-65535 in the OCR1A register will result in division factors of 2-131072.
- Timer/Counter1 counts clock pulses at input pin PD5 in CTC mode. The counter is cleared to zero and the output pin OC1A (PB3) toggles whenever the counter value matches the value in the OCR1A register. Values 0-65535 in the OCR1A register will result in division factors of 2-131072.

A Frequency Reference Using the ATtiny2313

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